Panel Fan-Out Manufacturing: Why, When, How?
The Jury Has Convened

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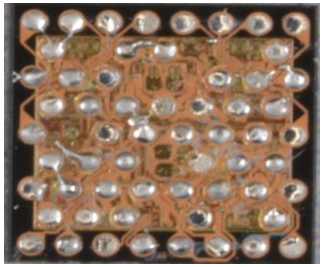
Example of FOWLPs in Smartphones

- **FO=WLPs$n$many$ Smartphones$**
  - Samsung'models'
  - Huawei'models'
  - Xiaomi'models'
- **Parts$from$Qualcomm$ using$eWLB$process$**

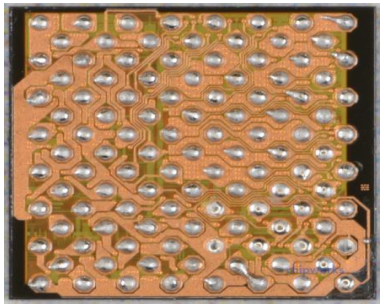
Qualcomm RF transceiver
Package is 3.3 mm x 3.3 mm



Source: ChipWorks.

Qualcomm PMIC
5.4 mm x 5.4 mm
part also found

Qualcomm Audio CODEC
Package is 4.25 mm x 3.90 mm

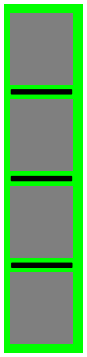
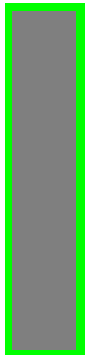
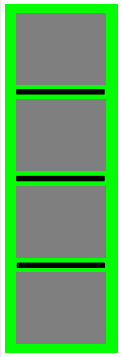
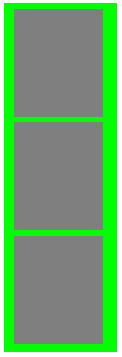
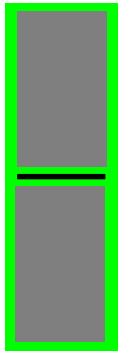
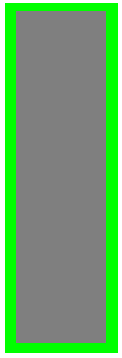
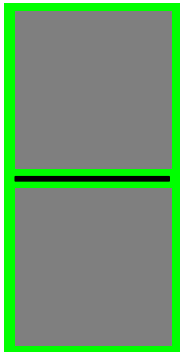


Source: ChipWorks.

Courtesy Jan Vardaman

Example of Scaling in Package Assemble

- Growth of Substrate Strips to Leverage Batch Processing Economics

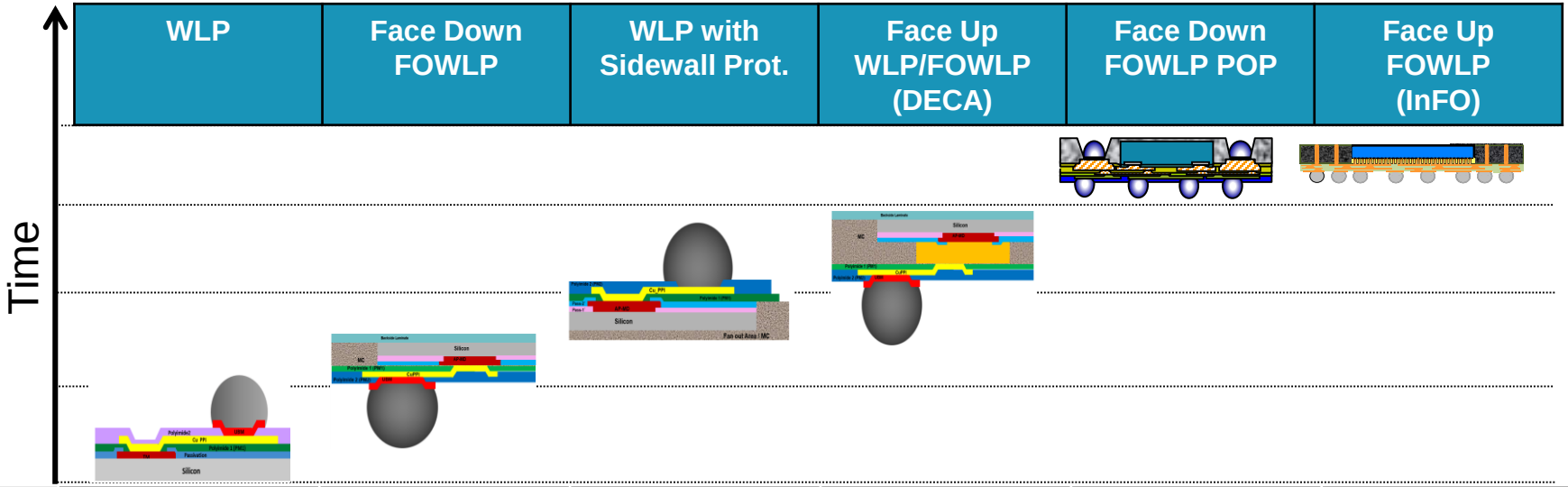
	Low Density		High Density				Ultra High Density 2-Up
	4-up	1-up	4-up	3-up	2-Up	1-up	2-Up
SAT							
A	62x230mm	-	-	74x240mm	-	-	95x240.5mm
B	63.45x240mm	63.45x240mm	-	-	-	72.6x240mm	
C	60x220mm	-	74x240mm	-	-	74x240mm	
D	63x240mm	-	-	-	-	73.6x241mm	

Packages per batch operation increasing,

➔ Utilization of Panel Increasing

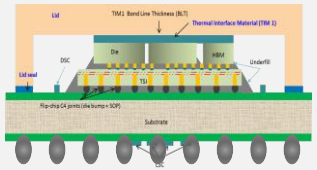
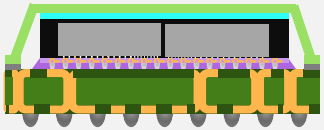
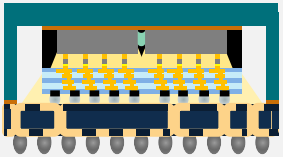
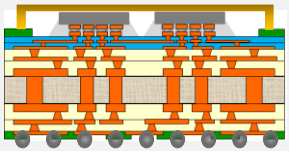
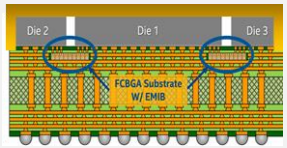
➔ Cost Advantage

Wafer Processed Package Evolution



	WLP	Face Down FOWLP	WLP with Sidewall Prot.	Face Up WLP/FOWLP (DECA)	Face Down FOWLP POP	Face Up FOWLP (InFO)
Features and Benefits	- Lowest cost solution if applicable - Finer pitch routing than substrates	- Cost effective for die requiring some fan out - Lower parasitics - Finer pitch routing than substrates	- More robust handling, Not prone to edge cracking	- Flat surface to pattern RDL. Finer pitch possible - Mold protection over die surface	- Thinner POP possible compared to substrate based	- Flat surface for patterning RDL. Finer pitch Pillars for POP connection than solder balls
Challenges	- Rel limits die size - Handling issues for EMS - Low K challenged	- 2+ layers of RDL more expensive than substrate pkg.	- Increases cost over WLP	- Requires growth of Cu pillar on die	- Cost For 2+ RDL	- Cost for 2+ RDL - Cost to grow Cu pillars for POP
Applications	- Devices that I/O boundary	- Alternative to FC for many apps - Multi chip modules	- Same as WLP	- Same as FOWLP, WLP, sidewall protected WLP	- Apps processor for high end phones	- Apps processor for high end phones

2.1/2.5D Advanced Packages for Multichip, Processors, GPUs and FPGA – Opportunities for FO Packaging

	2.5D			2.1D	
	TSI CoWoS, CoW, CoS	**FOCoS Fan Out Chip on Substrate**	**SWIFT (Die last FO)**	**2.1D Photo-Defined Organic Interposer (POI)**	**EMIB**
					
Suppliers	TSMC, Multiple OSATS	ASE	Amkor	Shinko	Intel
Features	• Si Interposer • Glass Interposers for electrical performance by GaTech • Die first or last assembly depending on process flow • In LVM	• Die first face down FO construction • Leverages HVM processes of standard FOWLP but fine pitch RDL • In Dev. • Panel possible	• Die last • Conventional RDL • Die last assembly • AOI inspected RDL • In Dev. • Panel possible	• Advanced PID Substrate • Die last assembly • AOI Inspected RDL • In Dev. • Larger panel possible	• Si Bridge Embedding • Laser SRO/ Mixed Bump • Known Good Si Bridge • Combination of 300mm and larger panel • In LVM
Assembly Complexity	Si Interposer +Substrate Assembly	FO processes+ PKG to Substrate Assembly	RDL+ Chip Joining + PKG to Substrate Assembly	Conventional Chip Joining only	Conventional Chip Joining only

FOWLP and the Quest for Smaller Form Factor, Higher Integration, and Larger Panels

- Eliminates die interconnect (bump & wire bonds) and substrate
  - Finer pitches than substrate based technology
  - 10-15um L/S common, 5/5um in HVM, ~2/2um L/S in LVM
  - Shorter interconnects = Lower parasitic
  - Eliminate interconnect stress and ELK crack delamination issues
  - Can improve thermal characteristics
- Batch packaging process like WLP
  - Can use KGD
  - Round panels can leverage WLP and FC bumping equipment
  - Square panels can leverage material and process understanding form WLP
- Potential SiP, Multi-die, 3D Solution
- Larger panel batch processing in development to lower cost
  - Challenges in patterning, sputtering, plating, and materials
  - Challenges with metrology over large format